



Atty. Dkt. No. 045054-0158

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Hitoshi IRINO  
Title: SEMICONDUCTOR PROTECTION ELEMENT,  
SEMICONDUCTOR DEVICE AND METHOD FOR  
MANUFACTURING SAME  
Appl. No.: 10/796,999  
Filing Date: 03/11/2004  
Examiner: Lee, Calvin  
Art Unit: 2818  
Confirmation No.: 4645

**REQUEST FOR CLARIFICATION**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

We have recently received the Notice of Allowance in the above-identified case. In reviewing form PTOL-37, the undersigned notes that the number of allowed claims is stated as 1-41. However, the number of claims allowed should be Claims 1-16 and 26-41.

Therefore, it is requested that the Examiner issue a corrected form PTOL-37 indicating that the number of allowable Claims in this application is 32, Claims 1-16 and 26-41.

Respectfully submitted,

Date January 19, 2006

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